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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of

Ritsuko Iwasaki

Serial No.: 09/496,421

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Group Art Unit: 2815

Examiner: Eugene Lee

For: SEMICONDUCTOR DEVICE HAVING AN IMPROVED LAYOUT PATTERN OF PAIR TRANSISTORS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUBMISSION OF CORRECTED FORMAL DRAWINGS

Sir:

Submitted herewith are corrected formal drawings for Figures 1-8 for the above-identified patent application, which incorporate the drawing changes approved by the Examiner on the Form PTOL-37, dated March 9, 2004. Approval and acknowledgment of receipt are respectfully requested.

Respectfully submitted,

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Date: 5/20/04

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